ABSTRACT

A cacheless computer system comprising a central processing unit (CPU) and a high speed transition buffer interacting with different computer system resources such as address controller, main semiconductor memory and input output devices by means of plurality of system buses. The transition buffer contains starting memory locations of each jump or branch location of the program. When a branch or jump instruction is encountered by the CPU, it fetches the starting locations from the high speed transition buffer executing at CPU speed. When multiple instructions are executed from the transition buffer, enough time is available to the address controller to access the remainder of the branch or jump program located on the slower, low power, low cost DRAM type memory. The program then continues to be executed from the parallel blocks of memory pre-fetched and available on parallel memory blocks without access time requirements until the program is completed or a next jump or branch instruction is encountered. The size of the program that can be executed without interruption can be the size of the entire main semiconductor memory. The system also works on multiprocessing system where cache coherency problems are eliminated. Time critical real time applications are more deterministic. Digital signal processors (DSP) for real time applications are able to implement larger programs without cache miss and latency problems. A new compiler is required to compile the program for the unique requirements of this architecture. Timing characteristics of the implementation is understood well in advance at the compile time.